Differential Circuits

The present invention relates to differential circuits. Such circuits are used in a wide range of electronic devices including, for example, active matrix display devices.

The conventional circuit symbol and graphical definition of a differential voltage comparator are given in Figures 1(a) and 1(b) respectively. The output voltage V_{OUT} is related to the two input voltages at nodes P and N (i.e. V_P and V_N) by:

$$\begin{cases} V_{OUT} = V_{DD} & \text{if } (V_P - V_N - V_{OS}) > V_{Sensitivity} \\ V_{OUT} = V_{SS} & \text{if } (V_P - V_N - V_{OS}) < V_{Sensitivity} \end{cases}$$

$$V_{SS} < V_{OUT} < V_{DD} \quad \text{if } |V_P - V_N - V_{OS}| < V_{Sensitivity}$$

where V_{DD} and V_{SS} are the voltages of the supply rails, V_{OS} is the input offset-voltage caused by non-ideal transistor characteristics, and $V_{Sensitivity}$ is the minimum difference between input voltages before a full output swing (V_{DD}-V_{SS}) can occur.

A conventional differential voltage comparator consists of two stages of amplifiers, as is well known in the art. It consists of a differential amplifier circuit as shown in Figures 2 and 3 to perform an amplification of the voltage difference between its two inputs V_P and V_N. For optimum operation, a pair of input transistors T_3 and T_4 identical in characteristics are required to connect to a pair of identical current-mirror transistors T_1 and T_2. In figure 2 the inputs are NMOS and in figure 3 the inputs are PMOS.

In theory, transistors with the same channel width and length (W and L)

dimensions should behave identically. This is normally the case for single crystal technology. However, when the device feature size approaches the sub-micron level, spatial variation of transistor characteristics, although small in absolute terms, becomes a problem. This is because the variation becomes large in relation to the operating voltages. However, when the variation can be described by a linear function of position, this problem can be solved by choosing an appropriate topology for the transistors such that the effect of variation is averaged out. In the case of Thin Film Transistor (TFT) technology, the spatial variation of transistor characteristics is large (in absolute and relative terms) and is randomly distributed. The topological approach cannot be used. An object of the present invention is to solve this problem.

The effect of a random spatial variation of transistor characteristics on a conventional comparator circuit comprising a differential-pair is an unpredictable V_{os}. One proposed solution is to implement additional switches and a capacitor network for detecting and canceling any input offset-voltage V_{os} caused by the non-ideal transistor characteristics of the comparator circuit. This is effective, but it increases the component count.

Another solution is not to use a differential-pair. A charge-balance differential-voltage comparator requires only the matching of capacitances. Capacitances are easier to match than transistors.

A solution to solve the current-mirror pair problem is to use a single-transistor current-mirror as shown in Figure 4a. This circuit requires two non-

overlapping clock pulses Φ_1 and Φ_2 to operate. The input current I_{IN} sets the gate bias voltage V_{GS1} for transistor T_1 when the switches S_1 and S_2 are turned on. This bias condition is stored across C_1 and mirrors the I_{IN} as output current I_{OUT} on T_1 when S_3 is turned on. Figure 4b explains the operation graphically. The current level at point A when Φ_1 is high is similar to the current level at point B when Φ_2 is high (i.e. $I_{OUT} \approx I_{IN}$), thus achieving the current-mirror function. In the illustrated circuit the load is a passive device.

According to the present invention a single transistor current-mirror is interfaced with a suitable load in combination with a suitable set of switches to accomplish a comparator function. The comparator function is, thus, not influenced by the spatial distribution of transistor characteristics.

Embodiments of the present invention will now be described by way of further example only and with reference to the accompanying drawings, in which:-

Figures 1(a) and 1(b) show the conventional circuit symbol and graphical definition of a differential voltage comparator, respectively;

Figure 2 shows the input stage of a conventional comparator circuit using a differential pair with NMOS inputs;

Figure 3 shows the input stage of a conventional comparator circuit using a differential pair with PMOS inputs;

Figures 4(a) and 4(b) respectively show a single transistor current-mirror and a graphical description of the operation of that circuit;

Figures 5(a) and 5(b) respectively a circuit according to an embodiment of the present invention and a graphical representation of the operation of that circuit;

Figure 6 symbolically illustrates the internal mechanism of a differential comparator according to an embodiment of the present invention;

Figure 7 shows the driving waveform of the circuit of figure 6;

Figure 8 illustrates a circuit according to an embodiment of the present invention;

Figure 9 illustrates a circuit according to another embodiment of the present invention;

Figure 10 illustrates a circuit according to a further embodiment of the present invention;

Figure 11 illustrates the interface of the circuit of one of the embodiments with a following stage in an electronic device;

Figure 12 illustrates another example of the interface of the circuit of one of the embodiments with a following stage in an electronic device;

Figure 13(a) illustrates another embodiment of a circuit according to the present invention and figure 13(b) shows the driving waveforms for that circuit;

Figure 14 illustrates a modified form of the circuit of figure 8;

Figure 15 shows simulation results for the circuit of figure 9;

Figure 16 is a symbolic representation of a differential comparator according to the present invention including an output stage;

Figure 17 is a variation of figure 16;

Figure 18 is a detailed diagram of a circuit in accordance with the present invention;

Figure 19 is a circuit diagram illustrating the input stage of an active matrix sensor cell;

Figure 20 is a circuit diagram illustrating a current sensor having a discriminator circuit and an output stage;

Figure 21 is a block diagram useful in explaining the driving method of a multiplexed current sensor for use in a finger print sensor; and

Figure 22 is a timing diagram of a multiplexed current sensor for use in a finger print sensor.

Embodiments of the present invention will now be described in relation to a differential-current comparator circuit. A method of converting this circuit to a differential-voltage comparator will be described subsequently.

A circuit according to an embodiment of the present invention is illustrated in figure 5a. A single-transistor current mirror comprises a transistor T_1 with a capacitor C_1 connected between the source and gate thereof and a switch S_3 connected between the gate and the drain thereof. The switch S3 is operated by a control signal. The single-transistor current-mirror circuit is connected to two current sources that sink I_{REF} and I_{SEN} through switches S_{10} and S_{11} driven by two non-overlapping clock signals Φ_1 and Φ_2, respectively. The control signal to the single-transistor current-mirror circuit is connected to Φ_1. The output of this circuit is at node C, and the voltage at

this node is referred to as V_C.

The operation of this circuit is as follows.

Step 1:

Φ_1 goes high while Φ_2 remains low. Switches S_3 and S_{10} are now closed. This allows I_{REF} to flow through the diode-connected transistor T_1 and causes a voltage (equal to V_{GS1}, the gate-source voltage of transistor T_1) to appear across the capacitor C_1. The value of C_1 and the on-resistances of switch S_3 dominate the charge-up time. At the end of this cycle, V_C settles at a voltage V_{C1}.

Intermediate Step:

Both Φ_1 and Φ_2 are low. All switches are opened. Both current sources are disconnected from the single-transistor current-mirror circuit. The output voltage V_C is floating, or is determined by discharging through the output load (not shown) connected to node C.

Step 2:

Φ_2 goes high while Φ_1 remains low. Switch S_{11} is closed. The circuit is now configured as a source-follower amplifier with a current-source load. The output voltage is determined by the current source I_{SEN}. As shown in Figure 5b, at steady-state, if $I_{SEN} = I_{SEN2}$,which is greater than I_{REF}, V_C will be less than V_{C1}. However, if $I_{SEN} = I_{SEN1}$, which is less than I_{REF}, V_C will be greater than V_{C1}.

Figure 6 shows a symbol for this differential-current comparator circuit with

voltage output. The required driving waveform is given in Figure 7.

Figure 8 illustrates a specific example embodiment for the basic schematic as shown in Figure 5a. The switches S_3, S_{10} and S_{11} in Figure 5a are replaced with n-channel transistors T_3, T_{10} and T_{11}, respectively. P-channel transistors, in principle, can also be used, but n-channel transistors are preferred because they have a lower on-resistance and hence smaller transistor sizes will be needed. As a result, the voltage feed-through effect of Φ_1 and Φ_2 into nodes C and M is reduced.

The implementation of the current sources depends on the actual applications. One or both of them can be implemented as independent transistors, such as T_{12} and T_{13} in Embodiment 2 as shown in Figure 9, biased to operate in the saturation region. In Embodiment 2, voltages V_P and V_N controls T_{12} and T_{13} to produce I_{REF} and I_{SEN}, respectively. Although the circuit looks like a differential-voltage comparator, care must be taken if it is used as one because the trans-conductance of transistors T_{12} and T_{13} may not have the same characteristic (although they are the same size). The circuit as shown in Figure 10 illustrates how the circuit can be used as a differential-voltage comparator. Transistors T_{12} and T_{13} are merged into a single transistor T_{14}, with its gate terminal connected to V_P or V_N via transistor switches T_{10} and T_{11}, controlled by Φ_1 and Φ_2, respectively.

The circuits illustrated in Figures 5a and 8 to 10 pre-amplify the difference between the input signals and pass the difference signal to the next stage. In order to further increase the output voltage swing and to make sure a minimum output load is attached to node C, a traditional MOS input amplifier (such as a single-ended source-

follower amplifier) can be used. This is shown in Figure 11. Alternatively, node C may be attached to another single-transistor current-mirror circuit for further amplification, as shown in Figure 12. Essentially, the node C is connected to the gate of a transistor T_{35} which is connected between VSS and the output of the second single transistor current mirror. In addition, with reference to figure 10 and as shown in Figure 13a, the basic circuit can be expanded by introducing additional transistor switches. In figure 13a, transistor T_{12} is connected between V_{BIAS} and the gate of transistor T_{14}. Additional non-overlapping clock pulses such as that shown in Figure 13b will also be required. In figure 13a; Φ_1 is applied to the gate of T_{12}, Φ_2 is applied to the gate of T_{10} and Φ_3 is applied to the gate of T_{11}.

The circuits described above in relation to figures 5 to 13 can be modified to improve performance. When $\Phi 1$ goes down, the nodal voltage at nodes C and M are pulled down by the voltage feed-through effect at T_3 and T_{10}. Node C suffers the voltage feed-through effect from both T_3 and T_{10} and hence a greater disturbance results. This disturbance could lead to an unexpected output spike at the second comparator stage. To avoid this problem, additional transistors T_6 and T_7 may be introduced to isolate node C from transistor T_1. The circuit of figure 8 modified in this way is illustrated in figure 14. Additional transistors T_6 and T_7 are connected in parallel with each other and have their gates each effectively connected with a respective one of the two current source switches (T_{10} and T_{11}), so as to receive the respective drive signal (Φ_1 and Φ_2) applied to the current source switches.

Simulation results for the circuit as shown in Figure 9 with this modification

added are shown in Figure 15, with the circuit using polysilicon TFTs. V_C falls during the falling edge of Φ_1, but rises by the same amount during the rising edge of Φ_2, therefore the initial operating point of V_C during Φ_2 is unaffected.

Figures 16 and 17 illustrate schematically how the input stage can be interfaced to a subsequent stage. Figure 18 is a detailed circuit diagram of the input and self-bias comparator, in accordance with a preferred example of the present invention. The first stage of the circuit is exactly the circuit of figure 14. The output node C is connected to the input of a self bias comparator, the body of which comprises transistors T_2, T_4, T_5, T_{12}, T_{13}, T_{14} and T_{17} together with capacitors C_2 and C_3. The output stage of the self bias comparator comprises transistors T_8 and T_9. Node C is connected to the source of both of transistors T_4 and T_{12}. The drains thereof are respectively coupled through capacitors C2 and C3 to the respective gates of T_2 and T_{17}. The drains of T_4 and T_{12} are also respectively connected to the source of T_5 and T_{13}. The drain of both T_5 and T_{13} are both connected to VSS. Control signal Φ_1 is applied to the gates of T_4 and T_{13}. Control signal Φ_2 is applied to the gates of T_5 and T_{12}. The gates of T_2 and T_{17} are connected to each other and to the source of a transistor T_{14}, whose drain is connected to the source of T_{17} and whose gate receives signal Φ_1. The source of T_2 is connected to VDD and it's drain is connected to the source of T_{17}. The drain of T_{17} is connected to VSS. The interconnection of the drain of T_2 and the source of T_{17} provides the output to the gates of both T_8 and T_9. The source of T_8 is connected to VDD. The drain of T_9 is connected to VSS and the interconnection between the drain of T_8 and the source of T_9

provides the final circuit output.

This invention can be used in detecting the peak and valley in a fingerprint sensor. An example of a fingerprint sensor circuit is shown in Figure 19. The current source for I_{SEN} is the output signal from a sensor pixel of an active matrix sensor array. Thus, comparing figure 19 with figure 14 it will be seen that the reference current source is provided by transistor T_{20}, whose gate receives a voltage V_1, and that the sensing current source is provided by transistor T_{21}, whose gate receives a voltage V_2. Respectively between T_{20} and T_{10} and between T_{21} and T_{11} are active matrix selection switches T_{15} and T_{18}, and, T_{16} and T_{19}. When the sensing cell is selected the voltage VDD is applied to the gates of all of transistors T_{15}, T_{18}, T_{16} and T_{19}.

Figure 20 shows an embodiment of a current sensor circuit having a self-bias charge-balance comparator as the output stage. The input stage is the circuit of figure 19 and the same self bias comparator as shown in figure 18 forms the output stage. The driving scheme is shown in Figure 21. A non-overlap waveform generator outputs Φ_1 and Φ_2 which are applied as inputs to a first and second current sensor as well as to a multiplexor and latch circuit. The two current sensors receive an input current I_{in} and have their respective outputs connected to the multiplexor and latch circuit. The output of the multiplexor and latch circuit is fed through an output buffer stage so as to provide the final circuit output. The timing diagram for the circuit explained in figures 20 and 21 is shown in Figure 22.

The aforegoing description has been given by way of example only and it will be appreciated by a person skilled in the art that modifications can be made without departing from the scope of the present invention. For example, in figure 20 if the P type transistors are replaced by N type transistors and visa versa then V_{DD} becomes Vss and Vss becomes V_{DD}.